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Electrostatic clamp and method.

Abstract:

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(54) Elctrostatic clamp and method.

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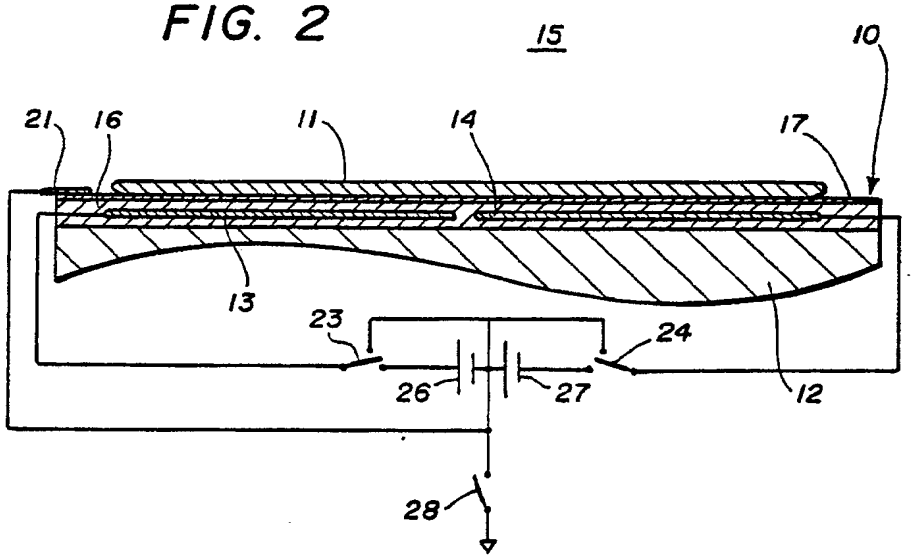
FIG. 2



EP 0 439 000 A1

ELECTROSTATIC CLAMP AND METHOD

Field of the Invention

The present invention relates to electrostatic clamps and, in particular, to the use of electrostatic clamps to hold workpieces such as semiconductor wafers on supports such as pedestals in plasma processing reactors.

Background of the Invention

The available techniques for holding wafers on pedestals or other supports in semiconductor wafer plasma processing reactors include mechanical clamping, vacuum clamping and electrostatic clamping.

Vacuum clamps are ineffective at the relatively high vacuum levels useful in present and future reactors.

Mechanical clamping involves clamping the wafer against the support using a peripheral ring or fingers. While mechanical clamps are effective under vacuum conditions, they have a number of shortcomings. For example, the movement of mechanical tooling can generate particulates, as can the contact between the mechanical clamps and the wafer surface. Furthermore, clamps shadow underlying regions of the wafer and may break or otherwise damage the wafer.

Also, the characteristics of the plasma are altered in the vicinity of clamps, thereby inducing process non-uniformity across the wafer and, in particular, at the edge of the wafer relative to the central portion. For example, etch rates may be reduced at the clamped edge of the wafer. This problem is exacerbated by the industry-wide practice of forming rectangular chips on circular wafers. To reduce wasted space, the chips are placed over the whole surface, including the areas very close to the edge of the wafer, that is, in the region affected by the plasma non-uniformities.

Electrostatic wafer clamps inherently do not suffer from the above-described problems. A typical electrostatic clamping design uses a pair of electrodes embedded in a dielectric matrix and biased oppositely and equally with respect to ground, for example, at ± 300 volts.

A representative multiple electrode pair type of electrostatic clamp is disclosed in U.S. Patent 4,184,188. That clamp includes a blade; a multiplicity of interleaved, positive and negative, paired electrodes which are arranged on the blade's surface; and a dielectric layer formed over the electrodes. When an electrically conducting wafer is placed over the electrodes and sufficient electrical potential is applied to the electrodes, negative charges in the wafer flow to the region of the wafer over the positively-charged electrode leaving positive charges on the wafer surface just over the negatively-charged electrodes.

The electrostatic fields and polarized charges associated with such clamps are shown in FIG. 1, which depicts a clamping structure comprising dielectric layers 1 and 2, positive and negative electrodes 3 and 4 embedded in layer 2, and wafer 11. The dielectric layers 1 and 2 provide electrical insulation between the conducting structures 3 and 4 (which are externally biased) and the wafer 11, and also increase the electric field, E_o, in the vacuum gap between wafer 11 and the upper dielectric layer 1. The clamping pressure, ^{P}clamp, can be calculated from the thickness of the dielectric layers, their dielectric constants, and the voltage, ^{V}clamp, applied to the clamp electrode(s). For this design, we assume that the clamp electrodes 3 and 4 are biased equally positive and negative with respect to the wafer surface's self-bias, so there is no net charging of the wafer when the clamp voltage is applied.

Referring further to FIG. 1, in general $E_i = E_1, E_2, \ldots E_n$ are the electric field strengths inside the respective dielectric layers $i = 1,2, \ldots n$, which have dielectric constants $k_i = k_1, k_2, \ldots k_n$ and thicknesses $t = t_1, t_2, \ldots t_n$. The value of E_n is E_o/k_n, where E_0 is the electric field in a microscopically thin vacuum gap between the bottom of the wafer 11 and the top surface of the upper dielectric layer 1. It can be shown that:

$$(t_1/k_1 + t_2/k_2 + \ldots + t_n/k_n)\, E_o = {}^{V}\text{clamp}, \qquad (1)$$

where ^{V}clamp is the electrical potential for either clamp electrode relative to the wafer.

Solving (1) for E_0 gives:

$$E_0 = V_{clamp/}\, (t_1/k_1, + t_2/k_2 + \ldots + t_n/k_n). \qquad (2)$$

The clamp pressure, P_{clamp} , is found using:

$$P_{clamp} = \sigma E_0, \quad (3)$$

where σ is the surface charge density (coul/m^2 in mks units) on the bottom of the wafer 11, or equally, that on the upper surface of the conductors 3 and 4 in the clamp. The charge density is found by using Gauss' law, which yields:

$$E_0 = \sigma/\epsilon_0, \quad (4)$$

where ϵ_0 is the permittivity of free space, 8.8 x 10EXP-12 in mks units. For the illustrated case of a two layer dielectric with negligible vacuum gap we find by substituting σ from (4) into (3) and E_0^2 from (2) into (3):

$$P_{clamp} = \epsilon_0 E_0^2 = \epsilon_0 \left(\frac{V_{clamp}}{t_1/k_1 + t_2/k_2} \right)^2, \quad (5)$$

where $t_1 = x_1 - x_0$, the thickness of the top layer 1 of dielectric and $t_2 = x_2 - x_1$, for the second layer 2. The units of P_{clamp} are newtons/m^2 which are about 1.42 x 10^{-4} psi for each nt/m^2.

If, for example, t_1 = 0.03 mm (30μ) for an upper layer of Al_2O_3, for which k_1 = 9 and t_2 = 0.1 mm (100μ) for lower layer 2 of TiO_2 which has $k_2 = 60$, then from (5): $P_{clamp} = 3.5\ V^2_{clamp}$ (nt/m^2) $\approx 5.10^{-4}\ V^2_{clamp}$ (psi).

Thus, a clamping voltage of 100 volts would produce about 5 psi clamping pressure (5.10^{-4} x (10^2)^2). If, due to a dust particle or surface irregularity there were to be a 1μ vacuum gap added, it would reduce the pressure by about thirty percent (30%) in the region where the gap is, as can be easily shown from equation 5.

As shown above, in both the single and the multiple pair clamps, the resulting clamping pressure, P_{clamp} , is directly proportional to the electrostatic forces acting upon the wafer. Specifically, this force is directly proportional to the square of the applied voltage, V_{clamp} , and the square of the dielectric constant, k_i, and inversely proportional to the square of the dielectric layer thickness, t_i. Quite apparently, the relationship evidenced in equation (5) provides motivation for using a thin, large k dielectric, if possible. This pressure, P_{clamp} , is applied without in-vacuo moving mechanical parts and without mechanically contacting the workpiece or disturbance of the plasma. However, such electrostatic clamping techniques have a number of important design and operational requirements, and potential shortcomings, which are summarized below.

1. Uniform Clamping Forces

First, a sufficient, uniform clamping pressure must be sustainable so that the wafer or workpiece is securely held flat, to provide uniform power deposition, and so that heat transfer is uniform to the underlying chuck or pedestal. During plasma operation, however, the plasma electrically charges and thereby biases the wafer potential negatively, with the result that the potential difference and the associated clamping force between the negative electrode and the wafer are decreased, while the potential difference and clamping force between the positive electrode and the wafer are increased. The obvious result is uneven clamping force, non-uniform inadequate thermal conduction between the wafer and the pedestal (conduction is the primary mode of wafer cooling in a vacuum) and, thus, non-uniform inadequate cooling and non-uniform processing.

2. Voltage Drop Across High Resistivity Dielectrics

Secondly, the clamp structure should not have a substantial impedance to rf power penetration because the associated voltage drop increases power dissipated in the impedance match network and the voltage required to sustain an rf discharge in which the wafer-holding electrode is powered. Typically, as described

above, wafers are supported on one of the rf electrodes on which the electrostatic clamp is formed or attached. RF current (i. e., displacement current) must be conducted through the clamp dielectric to the plasma in order to complete the rf circuit. The dielectric must also have a relatively high dielectric strength in order to withstand the high electric fields associated with the clamping voltage of several hundred volts and the power surges and transients which might occur, e . g., where the clamping circuit is switched on. It can be shown that the high rf impedance of thick dielectrics typically used in electrostatic clamping causes a substantial voltage drop. For example, for Al_2O_3 or similar dielectric about 8-10 millimeters thick, having a dielectric constant, k, of about 10, and ϵ_0 about 8.8×10^{-12}, the resulting rf voltage drop at 13.56 MHz can exceed 100 volts. In short, the use of a relatively thick dielectric results in a relatively large voltage drop associated with the rf current through the dielectric, and requires the application of a commensurately higher voltage, and thus higher current through the stray capacitance of the powered electrode, to sustain the discharge at a given power level.

3. Release Time

Third, it is necessary that the surface charges responsible for the clamping force dissipate quickly, releasing the wafer from the clamp promptly after the clamping voltage is removed. However, electrostatic clamps or chucks often use a dielectric having a high resistivity, of the order of or greater than 10^{15} ohm centimeters. As a result, after the applied clamping voltage is turned off, perhaps thirty seconds elapse before the surface charge dissipates sufficiently that the wafer is released from the clamp. This delay reduces reactor throughput.

Summary of the Invention

Objects

As implied by the above discussion, it is a primary objective of the present invention to provide an electrostatic clamp which is useful in a plasma processing environment, and which clamps the workpiece to the associated support with a force which is uniform in time and space.

It is a second, related objective of the present invention to provide a clamp structure as described above in which the impedance to rf power penetration is substantially reduced from the levels seen in prior designs such as those discussed above.

It is another, related objective of the invention to provide an electrostatic clamp having a dielectric with reduced resistivity, so that the surface charges responsible for the clamping force dissipate quickly after the clamping voltage is removed, allowing quick release of the wafer from the clamp.

It is yet another objective of the present invention to provide an electrostatic clamp structure which has a multiple layered dielectric to provide both resistance to electrical breakdown and to avoid exposing potentially contaminating materials to the plasma that could be a source of damage to the devices or circuits when the clamped workpiece is a semiconductor wafer.

Summary

In one aspect, the invention which accomplishes the above and other related objectives is embodied in an electrostatic workpiece clamp and its related method of use. The clamp is formed on a workpiece support in a plasma processing chamber, which comprises a pair of electrodes embedded in a dielectric material mounted or otherwise attached to the support; means for supplying positive and negative voltage to the respective electrodes; and an electrode exposed to the plasma and connected to the voltage supply means for applying the plasma voltage as reference voltage to the voltage supply means. Reflecting the fact that thicker dielectrics require higher clamping voltages and cause larger rf drops for a fixed rf current flow through the electrostatic chuck, preferably, the dielectric thickness is substantially less than 8 millimeters, causing an rf voltage drop across the clamp of substantially less than 100 volts. Typically, a thin dielectric also simplifies the task of cooling the wafer because heat can be conducted more readily through it once the heat is conducted from the bottom surface of the wafer to the top surface of the dielectric.

In another preferred aspect, the dielectric has a resistivity less than about 10^{12} ohm centimeter, for enhancing charge dissipation upon removal of the clamping voltage and thereby providing a wafer release time substantially less than 30 seconds.

In another specific aspect, my present invention is embodied in an electrostatic workpiece clamp

formed on a pedestal within a plasma processing chamber, comprising: at least one pair of generally flat semi-circular electrodes or conductors embedded in a dielectric and mounted in thermally conductive contact on the pedestal; a pair of series-connected power supplies for applying positive and negative voltages to the respective electrodes of the pair; and a reference electrode positioned within the plasma and exposed to the same plasma voltage as the wafer. The reference electrode is adapted for electrical connection between the two power supplies, to apply the plasma voltage level experienced by the wafer as a reference voltage to the positive and negative power supplies, thus biasing the clamping electrodes equally and oppositely.

In still another aspect, the invention relates to a method of clamping a workpiece on an electrode in a plasma processing environment, by placing the workpiece on an electrostatic clamp having at least a pair of conductors, and generating a plasma in the vicinity of the workpiece while applying voltages which are positive and negative (relative to the workpiece) to the associated conductors, for clamping the workpiece thereto and applying the surface potential of the workpiece as a common reference to the positive and negative voltages.

Brief Description of the Drawings

The above and other aspects of my invention are disclosed in the enclosed drawings in which:

FIG. 1 schematically depicts the electric fields associated with a two-dielectric-layer electrostatic clamp;

FIG. 2 schematically depicts the structure of the electrostatic clamp of the invention;

FIGS. 3 and 4 are, respectively, a plan view and a vertical section view taken in the direction 4-4 in FIG. 3, showing a preferred non-cooled embodiment of the electrostatic clamp of the invention; and

FIGS. 5 and 6 are, respectively, a plan view and a vertical cross-sectional view taken along the line 6-6 in FIG. 5, showing a preferred gas-cooled embodiment of the electrostatic clamp of the invention.

Detailed Description of the Preferred Embodiment(s)

According to one aspect of the invention, differences in the clamping forces exerted by the positive and negative electrodes of an electrostatic clamp are eliminated by the use of a circuit which incorporates a reference electrode on that portion of the pedestal or chuck that is exposed to the plasma. The reference electrode biases the positive and negative electrodes equally with respect to the wafer.

The biasing circuit, reference electrode and other features of the invention are depicted in FIG. 2, which shows a flat workpiece such as a semiconductor wafer 11 supported on an electrostatic clamp 10 formed on an rf powered metal electrode pedestal 12 situated in a low pressure plasma reactor chamber 15. The clamp 10 comprises a pair of generally semi-circular conductive metal electrodes 13 and 14 which are embedded in or coated with a high k (dielectric constant) electrically insulating material 16 and, optionally, a thin protective dielectric surface coating 17. The surface coating 17 preferably is formed of a material such as polyimid or Teflon™ which is very clean and does not introduce particulates into the process chamber environment.

Reference electrode 21 is formed of a conductor such as silicon or metal on a portion of the clamp 10 which is exposed to the chamber's plasma processing environment 15. As shown in FIG. 2, preferably the electrode 21 is positioned in proximity to the wafer 11. A pair of series-connected batteries or other DC power supplies 25,27 and switches 23,24 selectively apply the positive and negative voltages from the power supplies to the respective positive and negative clamping electrodes 13 and 14. Appropriate resistors, capacitors and inductors may be included to prevent rf voltage from the electrodes getting into the biasing circuitry and too rapid changes in electrode voltages. The reference electrode 21 is connected between the power supplies. By opening a switch 28 to disconnect the power supplies from system ground, the reference electrode applies the bias potential experienced by the surface of the pedestal and by the wafer as the reference voltage to the DC power supplies 26 and 27 ensuring that the positive and negative potentials applied to the electrodes have the same magnitude (e.g., 300 volts) relative to the outer surface of the clamp and the wafer.

In short, the reference electrode 21 maintains the same magnitude potential difference between the positive electrode and the wafer on the one hand and between the negative electrode and the wafer on the other hand, despite the existence and fluctuation of the plasma self-biasing voltage. As a consequence, the reference electrode ensures that the positive and negative electrodes exert equal clamping force. The resultant uniform clamping force across the face of the wafer tends to flatten the wafer 11 against the pedestal 12, despite deviations from planarity on the part of wafer, and enables uniform power deposition. Also, the uniform clamping force enables the uniform thermal conduction between the wafer and pedestal

which is so essential to adequate, uniform cooling of the wafer in the absence of gas cooling and, thus, uniform process characteristics.

Preferably, the dielectric material has a combination of (1) high dielectric strength to permit the use of a dielectric coating 16 which is very thin relative to the layers of dielectric typically used for electrostatic clamps and (2) high dielectric constant, to permit the use of low clamping voltages without compromising clamping pressure. (See Equation (5).)

One suitable dielectric material is the hard anodized aluminum coating material available under the trade name Magnaplate HCR™ from General Magnaplate. Magnaplate HCR™ anodized aluminum has a dielectric constant, k, of about 9. The use of such material permits the dielectric coating to be reduced to much less than 1 mm thickness, e.g., to be reduced to 0.05 mm. This reduces the rf voltage drop through the clamp from the underlying electrode from 100 volts to less than 1 volt and, thus, provides low impedance transmission of rf power through the clamp. The substantially reduced voltage drop results in a commensurate reduction in the voltage which must be supplied to the powered electrode in order to sustain the plasma discharge which reduces power loses in the impedance match network. The thin, high k dielectric also permits low d.c. voltages to be used for the offsets of the clamping electrodes while maintaining high clamping pressure (>1 psi).

Another suitable dielectric material is alumina porcelain such as Coors Porcelain AD94, which has a dielectric constant of approximately 8.9, very low dielectric dissipation (10^{-3}) and reasonable thermal conductivity (approximately 0.04 cal/cm^2/cm/sec/$^\circ$ C). The dielectric strength of this material is sufficiently high (approximately 600 volts/mil) that it can withstand many times the voltage experienced by the clamp. That is, it easily withstands transients and power surges.

Also, the thickness of the additional thin dielectric coating 17 can be tailored to provide a compliant, heat conductive heat transfer layer between wafer and E-chuck. With such a dielectric thickness, the clamp force is not significantly reduced by small gaps or particles. Thus, for a thickness of 0.15 millimeter (0.006 inch) of aluminum porcelain, a one micron gap between the wafer and the clamp caused by particulates or non-perfect planarity in the wafer results in only a six percent decrease in clamping pressure locally.

In addition, it was determined that the described anodized aluminum and porcelain ceramic materials can be doped with a few weight percent of impurities such as copper to reduce the usual resistivity from 10^{15}-10^{16} ohm centimeter to about 10^{12} ohm centimeter or less. This greatly accelerates surface charge dissipation and reduces the release time to a few seconds. Preferably, the doping is done by ion implantation of the formed dielectric coating(s) 16 or during formation of the coating(s), as by introducing an impurity during sputter coating of the dielectric.

Furthermore, the low dielectric resistivity permits a very low voltage to be maintained between the exposed clamp surfaces and the clamp electrodes when a wafer clamping voltage is not being applied or when a plasma cleaning process is being used, to minimize or prevent particle accumulation on the surface of the clamp.

FIGS. 3 and 4 depict a non-cooled embodiment 10A of the schematized version 10 of the electrostatic clamp shown in FIG. 1. The illustrated semi-circular electrodes 13 and 14 are conductors such as aluminum. In general, the opposite polarity electrodes may be of essentially any complementary configuration (such as interdigitated fingers) which have substantially equal areas and together occupy most of the clamp surface area. A coating of material such as the above-mentioned preferred Magnaplate HCR™ high k dielectric may be formed on the top and bottom surfaces of the clamp electrodes by anodization. (Alternatively, the dielectric can be deposited by sputter deposition.) The anodized electrodes may have holes formed therein, such as holes 31 for wafer support pins and holes 32 for bolting to the pedestal 12. Leads (not shown) are attached to the anodized electrodes at the periphery of the electrodes, and the electrodes may be placed in a frame 33 made of Ardel™ insulator (or other suitable insulator) such that the electrodes are flush with the top and bottom surfaces of the frame. As mentioned, the dielectric may be doped with an impurity such as copper, nickel, chromium, silicon, nitrogen, etc., either during the formation of the anodization or afterward by ion implantation, to reduce the electrical resistivity to about 10^{12} ohm centimeter or less. The preferred range of thicknesses using the Magnaplate HCR™ dielectric is 0.025 - 0.05 millimeters.

Forming the clamp as described above using the Magnaplate HCR™ dielectric material of thickness 0.025 mm on the top and bottom surfaces and forming a reference electrode of silicon or SiC on the outer/upper surface of the exposed surface
of the electrode, provides a clamping force of $\geq$ 1 psi for applied electrode clamping voltages < 100 volts and provides an rf voltage drop across the electrostatic clamp of < 1 volt. In addition, the release time is 1 - 3 sec.

FIGS. 5 and 6 depict an alternative version 10B of the electrostatic clamp, one which is designed for

gas cooling. In this illustrated case, the top dielectric layer 16A is formed with a plurality of annular, generally concentric raised areas 36 and 37 for the purpose of forming gas reservoirs behind the wafer. A circumferential gasket 38 provides a gas seal between the clamp and the wafer. (The seal need not be gas-impervious; in fact, it may be desirable to use process gas as the cooling gas and to bleed the process gas peripherally out from the wafer into the process chamber 15.) As illustrated schematically, process gas may be applied via suitable conduit(s) 39 in the pedestal 12 and the center hole 41 in the clamp to the interface between the wafer 11 and the clamp 10.

In view of the above-described preferred and alternative embodiments of the invention, those of usual skill in the art will readily derive other adaptations and embodiments which are within the scope of the appended claims.

Claims

1. An electrostatic workpiece clamp (10) suitable for a plasma processing environment (15), comprising: at least a pair of electrodes (13, 14; 13A, 14A) embedded in a dielectric material (16); means (23, 24, 26, 27) for supplying positive and negative voltage to the respective electrodes (13, 14); and an electrode (21) exposed to the plasma environment (15) and connected to the supply means (23, 24, 26, 27) for applying the plasma voltage as the reference voltage to the supply means.

2. The electrostatic clamp of claim 1, wherein the dielectric (16) thickness is substantially less than one millimeter for providing a low rf voltage drop across the clamp substantially less than 100 volts.

3. The electrostatic clamp of claim 1 or 2, wherein the dielectric (16) has a resistivity of about 10^{10} - 10^{12} ohm centimeter for providing a wafer release time substantially less than 30 seconds.

4. The electrostatic clamp of claim 1, 2, or 3, wherein the dielectric (16) has multiple layers to reduce contamination and aid heat transfer.

5. The electrostatic clamp of any preceding claim, wherein said electrostatic clamp (10) is formed on a pedestal (12) within a plasma-processing chamber (15) for holding said flat workpiece, such as a semiconductor wafer (11), on said pedestal, said electrodes are generally flat complementary-shaped electrodes or conductors (13, 14; 13A, 14A) embedded in said dielectric (16) and mounted in thermally conductive contact on the pedestal (12), said supply means is a pair of series-connected power supplies (26, 27) for applying positive and negative voltages to the respective electrodes (13, 14; 13A, 14A) of said pair, and a reference electrode (21) is positioned within the plasma at the same self-bias voltage as the wafer (11), the reference electrode (21) being adapted for electrical connection (23, 24) between the two power supplies (26, 27) for supplying the self-bias voltage on the wafer (11) as a reference voltage to the positive and negative power supplies (26, 27).

6. The electrostatic clamp of claim 5, wherein the two power supplies are batteries.

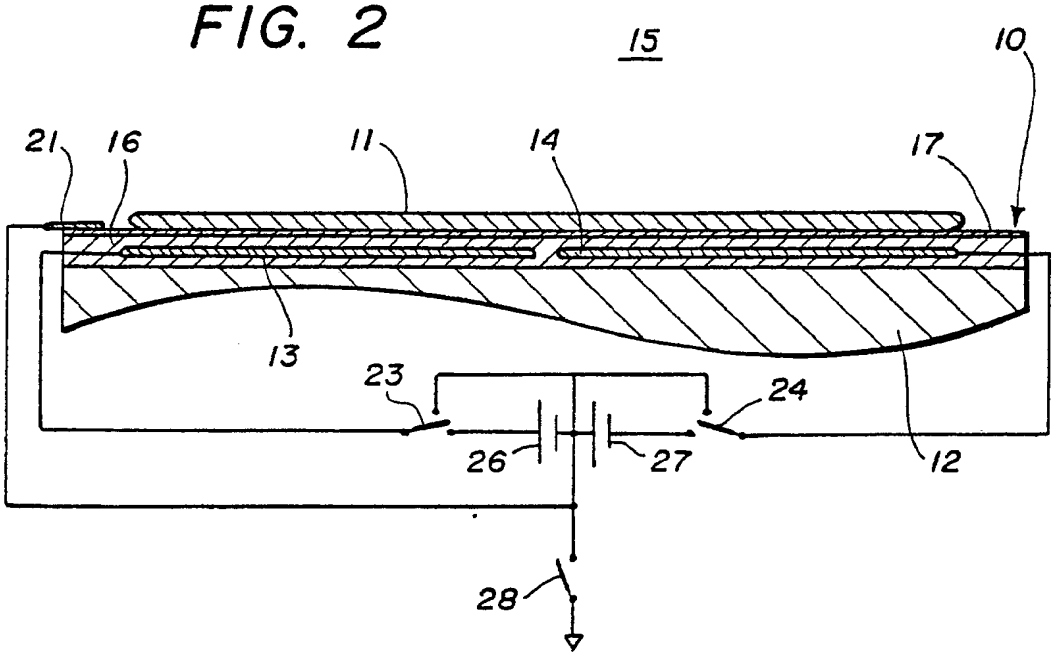
7. The electrostatic clamp of any preceding claim, comprising gas cooling means (39, 41).

8. The electrostatic clamp of claim 7, wherein a top layer (16A) of said dielectric (16) is formed with a plurality of annular, generally concentrically raised areas (36, 37) for forming cooling gas reservoirs behind said wafer (11).

9. A method of electrostatically clamping a workpiece in a plasma processing chamber (15) comprising: providing a clamp (10) having at least a pair of positive and negative conductors affixed to a support electrode (13, 14; 13A, 14A); and generating a plasma in the chamber (15) while applying relatively positive and negative voltages to the respective conductors for clamping the workpiece thereto and applying a plasma self-bias voltage proximate the workpiece as a common reference to the positive and negative voltages.

10. The method of claim 9, further comprising the step of cooling said clamp (10).

FIG. 2



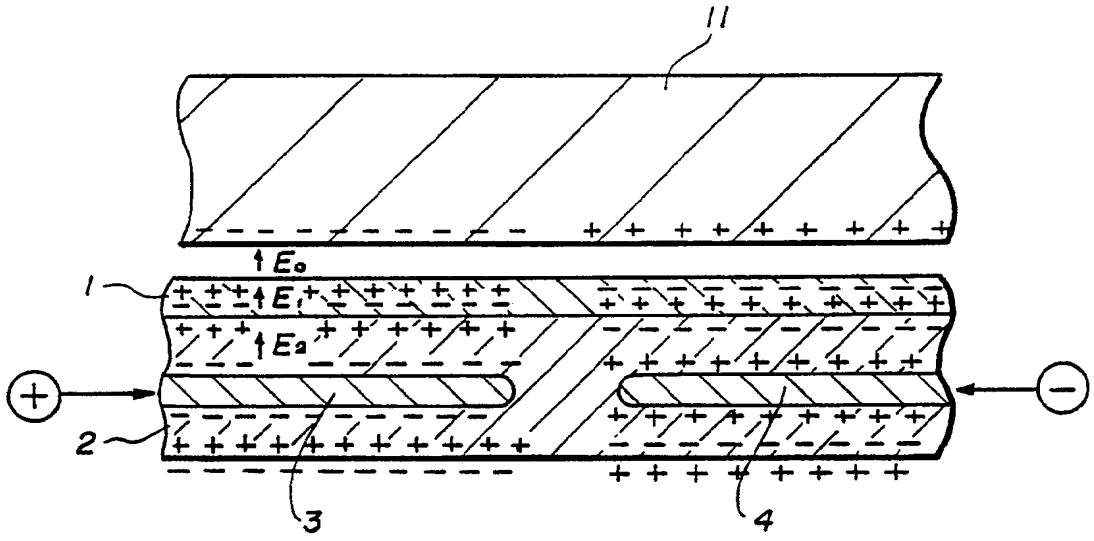
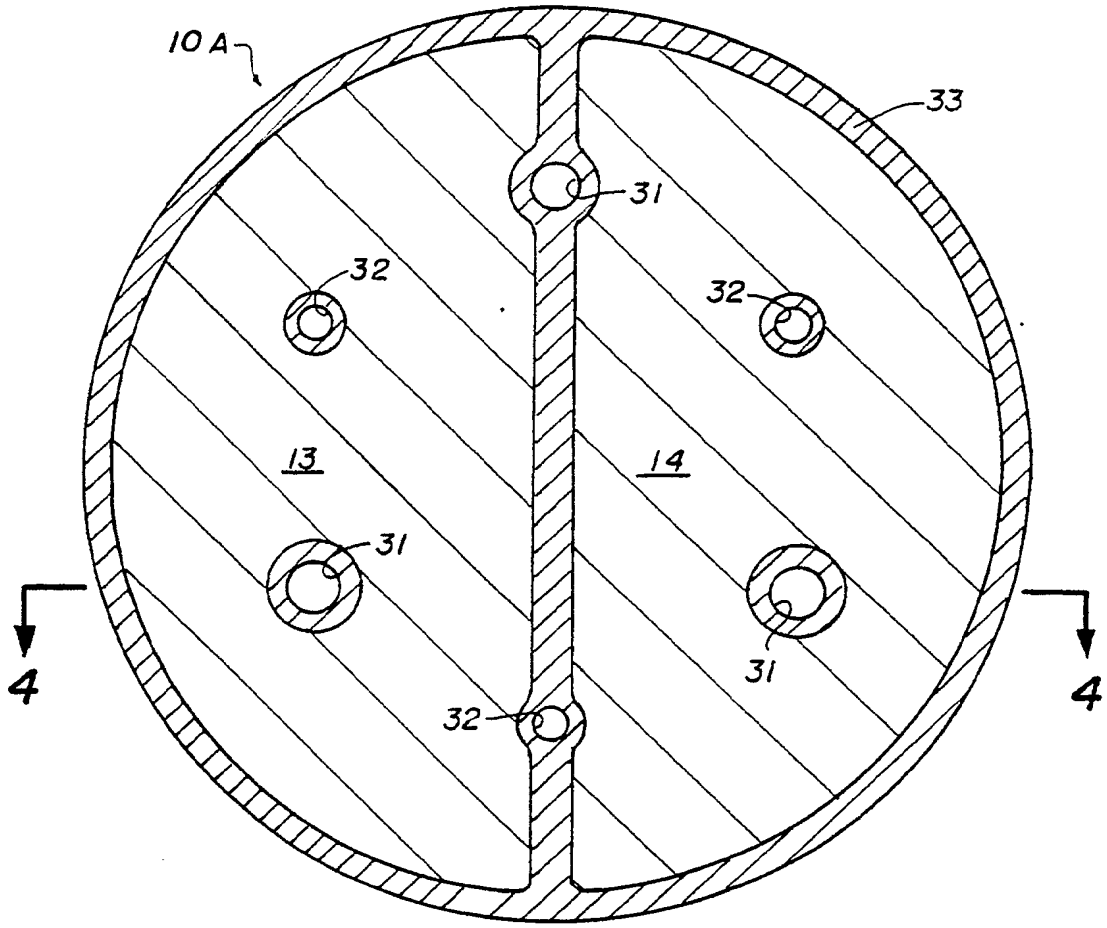


FIG. 1

FIG. 3



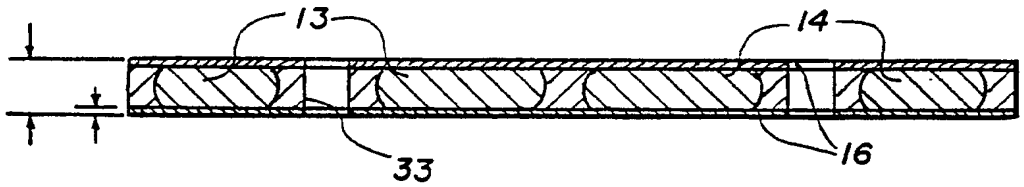
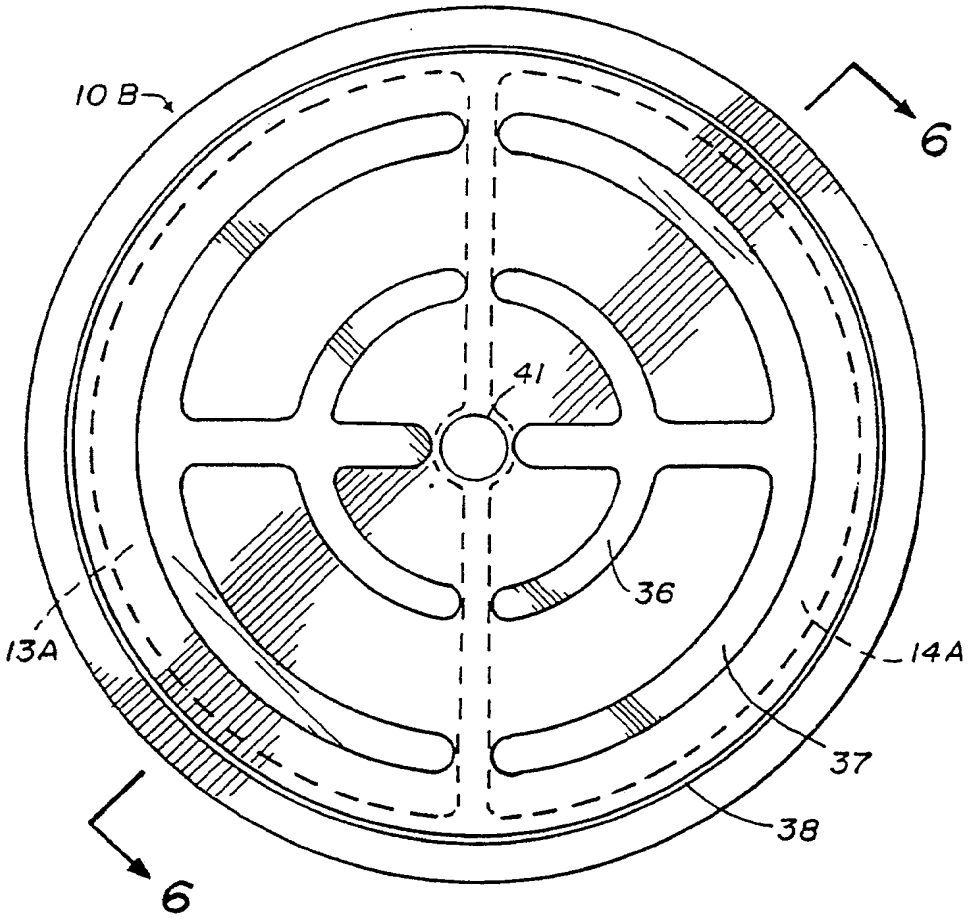


FIG. 4

FIG. 5



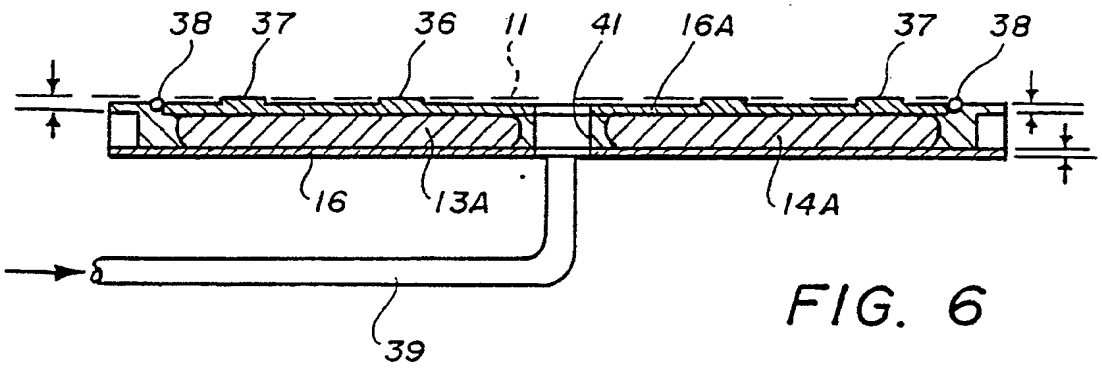


FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 10 0003

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A,D	WO-A-7 900 510 (VEECO INSTRUMENTS) * page 5, line 1 - page 10, line 3; figures 1-6 *	1,5,7,9,10	H 02 N 13/00 H 01 L 21/00
A	EP-A-0 171 011 (KABUSHIKI KAISHA TOKUDA SEISAKUSHO) * page 3, line 19 - page 8, line 6; figures 1-6 *	1,2,5,7,9, 10	
A	GB-A-1 443 215 (MULLARD) * figure 4 *	1	
A	US-A-4 671 204 (J.M.BALLOU) * abstract; figures 1, 4 *		

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
H 02 N H 01 L H 01 J

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	06 May 91	ZANICHELLI F.

CATEGORY OF CITED DOCUMENTS

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